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1. (AMENDED) An apparatus comprising:

a first circuit configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals; and

5 a second circuit configured to present said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

2. The apparatus according to claim 1, wherein said first clock signal comprises a bit clock signal.

3. The apparatus according to claim 1, wherein said second clock signal comprises a reference clock signal.

4. The apparatus according to claim 1, wherein said first circuit further comprises:

a third circuit configured to generate (i) one or more select signals and (ii) a selected clock signal in response to (i) 5 said first clock signal and (ii) a phase select signal.

5. The apparatus according to claim 4, wherein said first circuit further comprises:

a phase comparator circuit configured to generate said phase select signal in response to said one or more select signals
5 and one of said one or more serial data signals.

6. The apparatus according to claim 4, wherein said third circuit comprises a phase generation and select circuit.

7. The apparatus according to claim 4, wherein said first circuit includes a deserializer circuit configured to generate said parallel output data signal in response to said selected clock signal and another one of said one or more serial
5 data signals.

8. The apparatus according to claim 7, wherein said first circuit further comprises:

a multiplexer configured to generate (i) said one of said one or more serial data signals and (ii) said another one of said
5 one or more serial data signals, in response to said one or more serial data signals.

9. (AMENDED) A circuit comprising:
means for generating a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial
data signals; and

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5 means for generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

10. (AMENDED) A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

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(A) generating a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals; and

5 (B) generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal, wherein said first clock signal is configured to control said pulse width.

11. The method according to claim 10, wherein said first clock signal comprises a bit clock signal.

12. The method according to claim 10, wherein said second clock signal comprises a reference clock signal.

13. The method according to claim 10, wherein step (A) further comprises the sub-step of:

generating (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal
5 and (ii) a phase select signal.

14. The method according to claim 13, wherein step (A) further comprises the sub-step of:

generating said phase select signal in response to said one or more select signals and one of said one or more serial data
5 signals.

15. The method according to claim 14, wherein step (A) further comprises the sub-step of:

generating said parallel output data signal in response to said selected clock signal and another one of said one or more
5 serial data signals.

16. The method according to claim 15, further comprising the step of:

generating said one of said one or more serial data signals and said another one of said one or more serial data
5 signals, in response to said one or more serial data signals.

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Please add the following new claims:

17. (NEW) The apparatus according to claim 1, wherein said second circuit is configured to generate a plurality of said serial data signals.

A3 ~~18. (NEW) The apparatus according to claim 1, wherein said first circuit is configured to receive to a plurality of serial data signals.~~

19. (NEW) The apparatus according to claim 9, wherein said second circuit is configured to generate a plurality of said serial data signals.

20. (NEW) The apparatus according to claim 10, wherein said second circuit is configured to generate a plurality of said serial data signals.